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MOSCONE WEST CENTER
SAN FRANCISCO, CA, USA

Universal Chiplet Interconnect Express (UCIe)™ : An open industry standard approach driving innovations at package level

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Agenda

- Introduction to UCIe
- On-Package Interconnects: Opportunities and Challenges
- Universal Chiplet Interconnect Express (UCIe): An Open Standard for Chiplets
- On-Package Interconnect evolution at Intel
- Future Directions and Conclusions

UCIe™ Universal Chiplet Interconnect Express

120+ Member Companies and growing!

Board Members

Leaders in semiconductors, packaging, IP suppliers, foundries, and cloud service providers are joining together to drive The open chiplet ecosystem.

JOIN US!

Alibaba Group
AMD
arm
ASE GROUP
Google Cloud
intel
Meta
Microsoft
NVIDIA
Qualcomm
SAMSUNG
tsmc

UCIe Consortium is open for membership

- UCIe Consortium welcomes interested companies and institutions to join the organization at the **Contributor and Adopter level.**
- **UCIe** was founded in March 2022, incorporated in June 2022. Two levels of memberships: Contributor and Adopter
- **Contributor Membership**
  - Access the Final Specifications (ex: 1.0, 1.1, 2.0, etc.)
  - Implement with the IP protections as outlined in the Agreements
  - Right to attend Corporation trade shows or other industry events as determined by the Board
  - Participate in the technical working groups
  - Influence the direction of the technology
  - Access the intermediate (dot level) specifications
  - Election to get to the Promoter Class/ Board every year when the term of half the board completes
- **Adopter Membership**
  - Access the Final Specifications (ex: 1.0, 1.1, 2.0, etc.), but not intermediate level specifications
  - Implement with the IP protections as outlined in the Agreements
  - Right to attend Corporation trade shows or other industry events as determined by the Board

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Moore Predicted “Day of Reckoning”

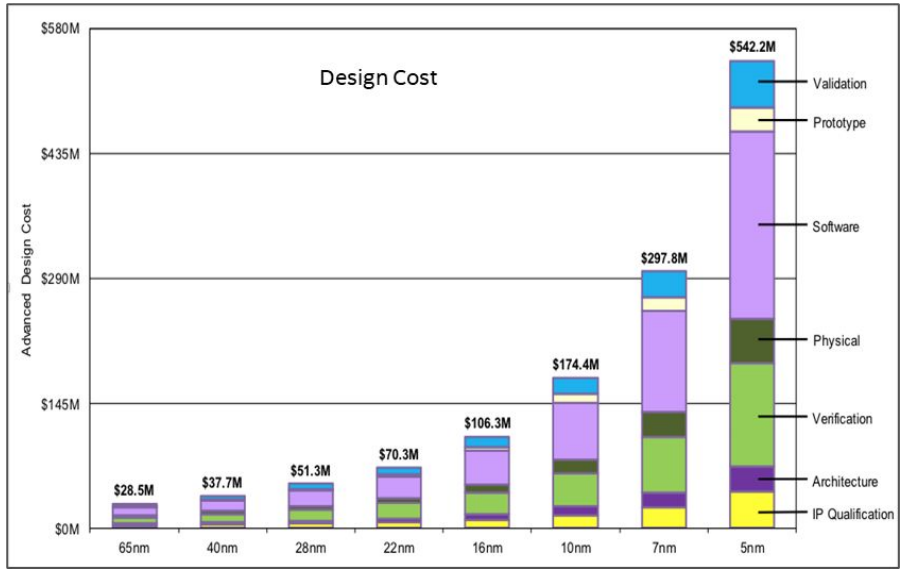
“It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected[1].”

-Gordon E. Moore

[1]: “Cramming more components onto integrated circuits”, Electronics, Volume 38, Number 8, April 19, 1965

Drivers for On-Package Chiplets

- Reticle Limit, yield optimization, scalable performance
  - Same dies on package (Scale-up)
- Increasing design costs at leading edge process nodes
  - Die-disaggregated dies across different nodes
  - Use new process node for advanced functionality
- Time to Market (Late binding)
- Custom silicon for different customers leveraging a base product
  - E.g., Different acceleration functions with common compute
- Different process nodes optimized for different functions
  - E.g., Memory, logic, analog, co-packaged optics
- High power-efficient bandwidth with low-latency access (e.g., HBM memory)



Source: IBS (as cited in IEEE Heterogeneous Integration Roadmap)

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Guiding Principles of UCIe

- Open Ecosystem with Plug-and-play
- Backward compatible evolution when appropriate to ensure investment protection
- Best power, performance, and cost metrics across the industry applicable across the entire compute continuum
- Continuously innovate to meet the needs of evolving compute landscape

(Leveraging decades of experience driving successful industry standards at the board level: PCIe, CXL, USB, etc.)

UCIe: Key Metrics and Adoption Criteria

Key Performance Indicators

- Bandwidth density (linear & area)
  - Data Rate & Bump Pitch
- Energy Efficiency (pJ/b)
  - Scalable energy consumption
  - Low idle power (entry/exit time)
- Latency (end-to-end: Tx+Rx)
- Channel Reach
  - Technology, frequency, & BER
- Reliability & Availability
- Cost: Standard vs advanced packaging

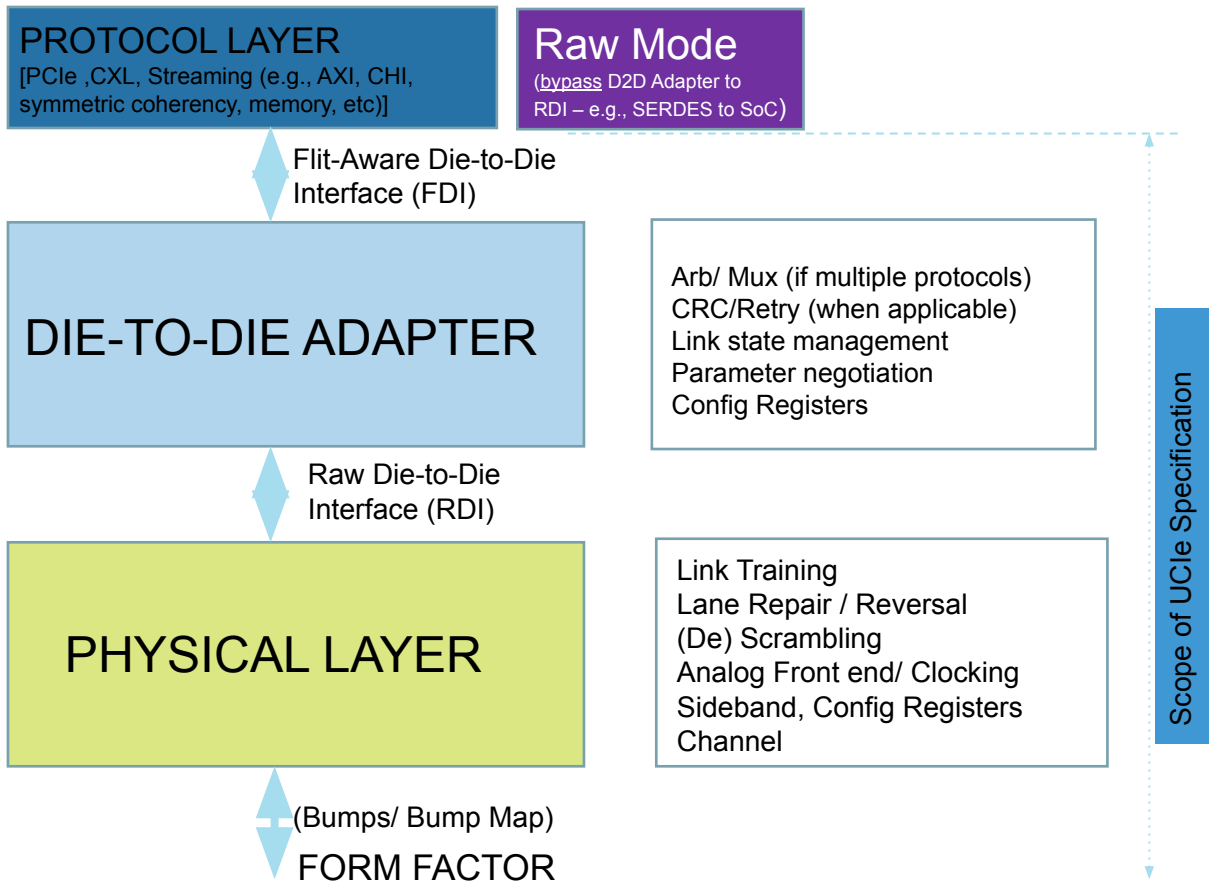
Factors Affecting Wide Adoption

- Interoperability
  - Full-stack, plug-and-play with existing s/w
  - Different usages/segments - ubiquity
- Technology
  - Across process nodes & packaging options
  - Power delivery & cooling
  - Repair strategy (failure/yield improvement)
  - Debug – controllability & observability
- Broad industry support / Open ecosystem
  - Learnings from other standards efforts

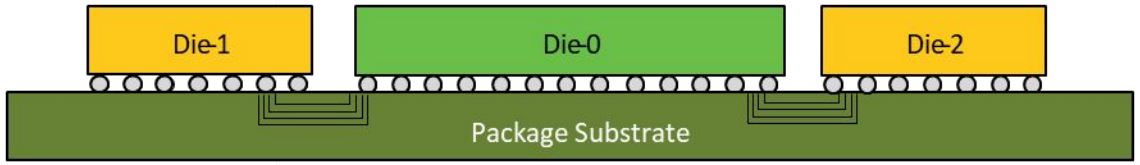
UCIe is architected and specified from the ground-up to deliver the best KPIs while meeting wide adoption criteria

UCIe 1.0 Specification

- **Layered Approach with industry-leading KPIs**
- **Physical Layer:** Die-to-Die I/O
- **Die to Die Adapter:** Reliable delivery
  - Support for multiple protocols: bypassed in raw mode
- **Protocol:** CXL/PCIe and Streaming
  - **CXL™/PCIe® for volume attach and plug-and-play**
    - SoC construction issues are addressed w/ CXL/PCIe
    - CXL/PCIe addresses common use cases
      - I/O attach, Memory, Accelerator
  - **Streaming for other protocols**
    - Scale-up (e.g., CPU/ GP-GPU/Switch from smaller dies)
    - Protocol can be anything (e.g., AXI/CHI/SFI/CPI/ etc)
- **Well defined specification**: interoperability and future evolution
  - Configuration register for discovery and run-time
    - control and status reporting in each layer
    - transparent to existing drivers
  - Form-factor and Management
  - Compliance for interoperability
  - Plug-and-play IPs with RDI/ FDI interface



UCIe 1.0: Supports Standard and Advanced Packages

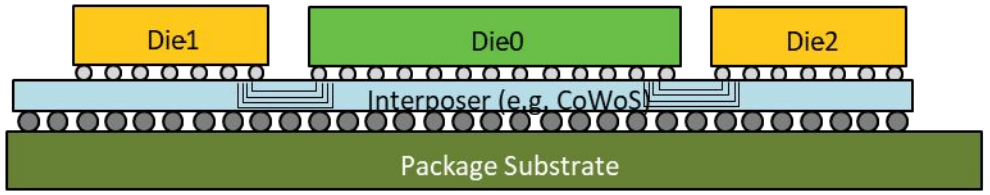


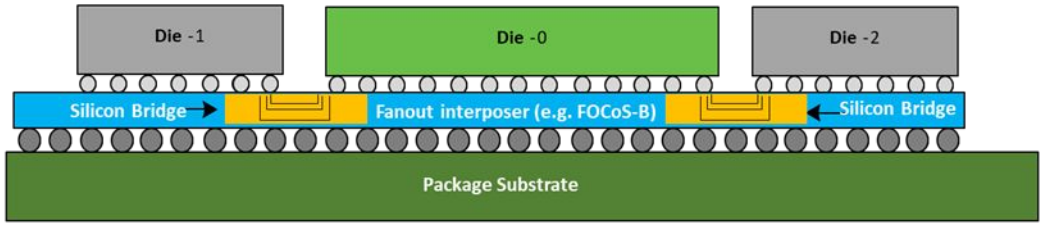
(Standard Package)

Standard Package: 2D – cost effective, longer distance

Advanced Package: 2.5D – power-efficient, high bandwidth density

Dies can be manufactured anywhere and assembled anywhere – can mix 2D and 2.5D in same package – Flexibility for SoC designer



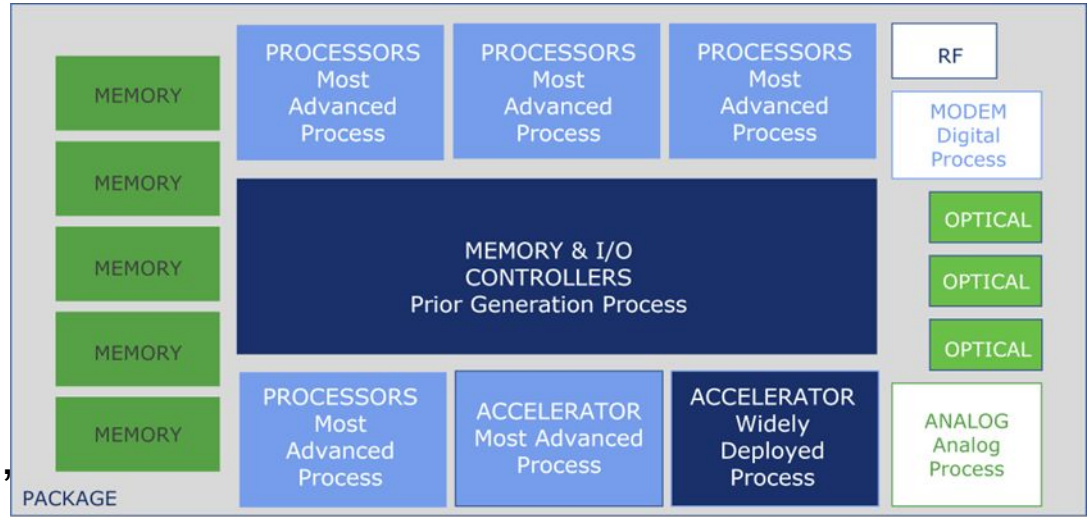


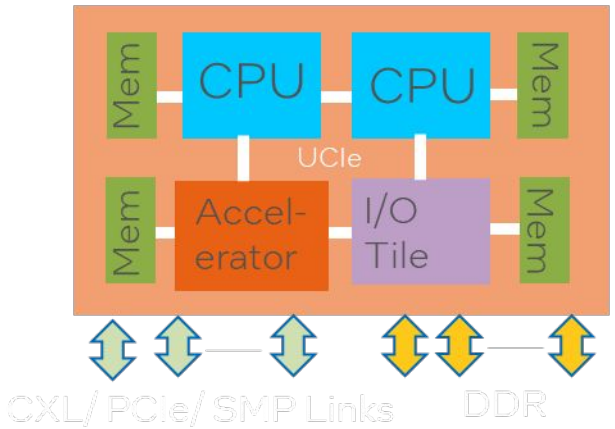
(Multiple Advanced Package Options)

- One UCIe 1.0 Spec covers both type of packaging options

UCIe Usage Model: SoC at Package Level

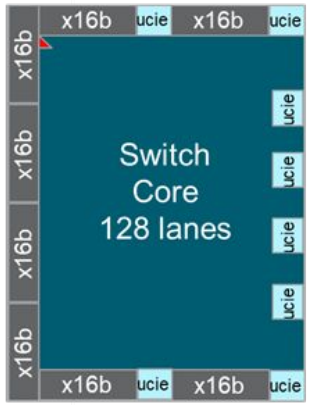
- SoC as a Package level construct
  - Standard and/ or Advanced package
  - Homogeneous and/or heterogeneous chiplets
  - Mix and match chiplets from multiple suppliers
- Across segments: Hand-held, Client, Server, Workstation, Comms, HPC, etc
  - Similar to PCIe/ CXL at board level



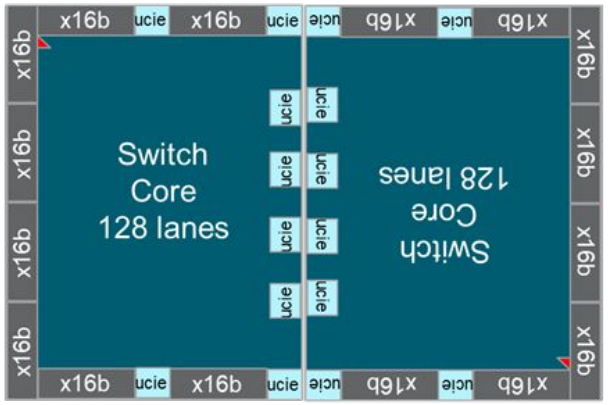


Example Scale-up SoC from homogeneous dies: Large Switch with on-die protocol as streaming over UCIe

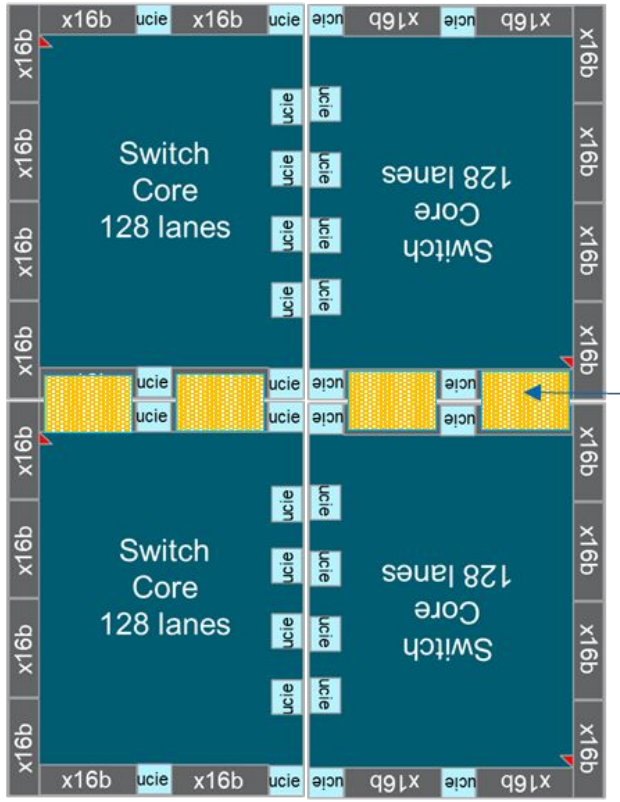
- Need large radix CXL switches – challenges: reticle limit, cost, etc.
- UCIe based Chiplets should help with scalable products
- 64G Gen6 x16b CXL links
- UCIe as d2d interconnect – while this is a scale-up CXL switch , a switch vendor may prefer to have their on-die interconnect protocol be transported over UCIe rather than create a hierarchy of switches which will not work for CXL 2.0 tree-based topology



Small CXL Switch (128 lanes)



Medium-sized CXL Switch (256 lanes)

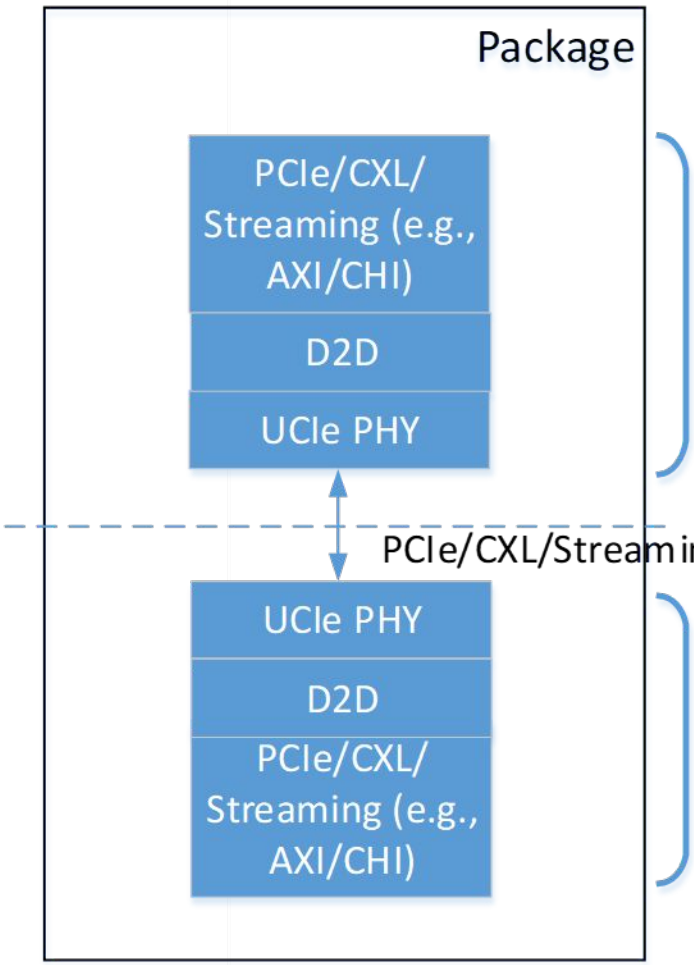


Large CXL switch (512 lanes)

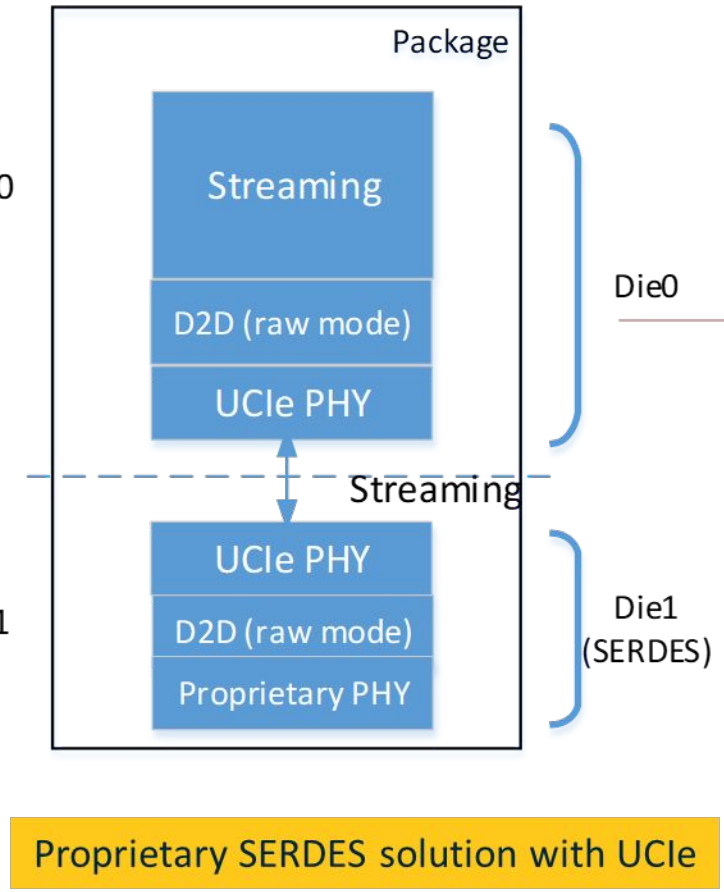
One can construct CPUs (low, medium, large core-count CPUs) from smaller dies connected through UCIe using the same principle
Here the UCIe PHY and D2D adapter will carry the packetized version of internal CPU interconnect fabric

Ack: Nathan Kalyanasundaram

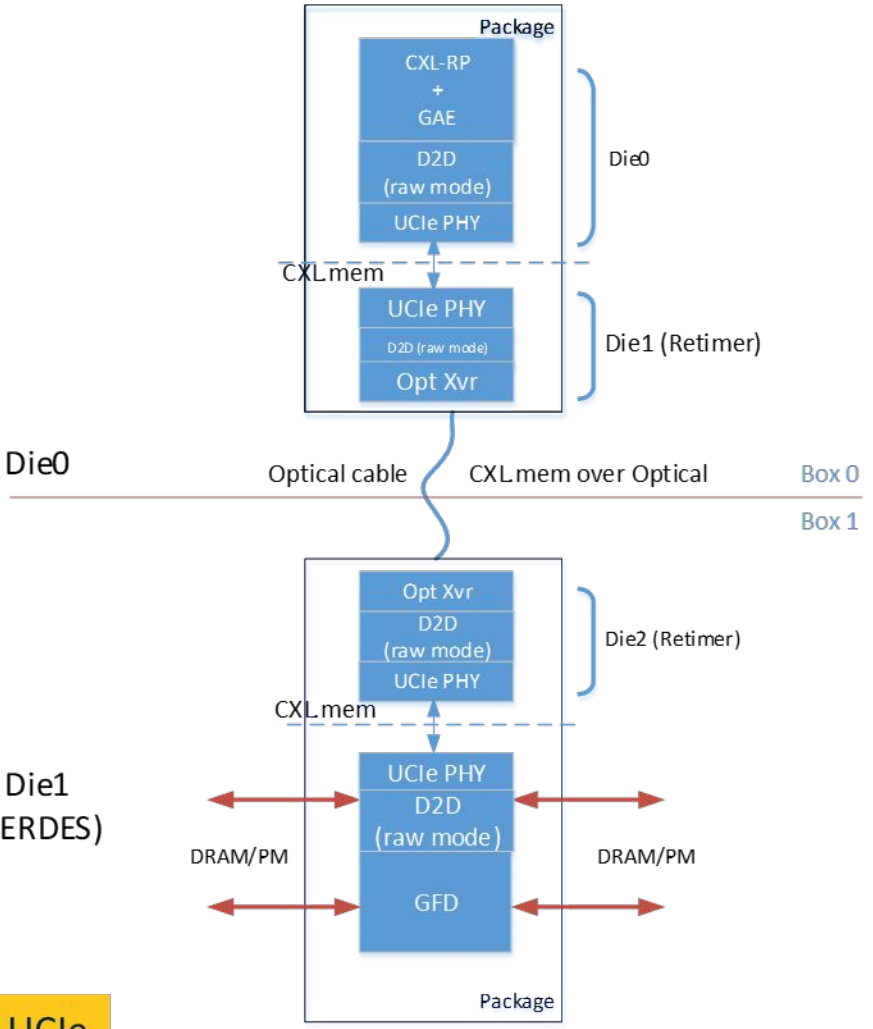
UCIe Based System TOPOLOGY: SOC as well as OFF-Package



Simple PCIe/CXL/Streaming over UCIe

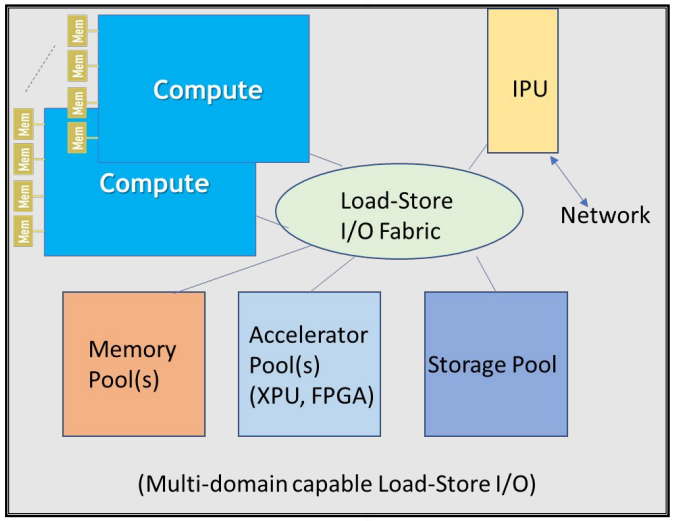


Proprietary SERDES solution with UCIe

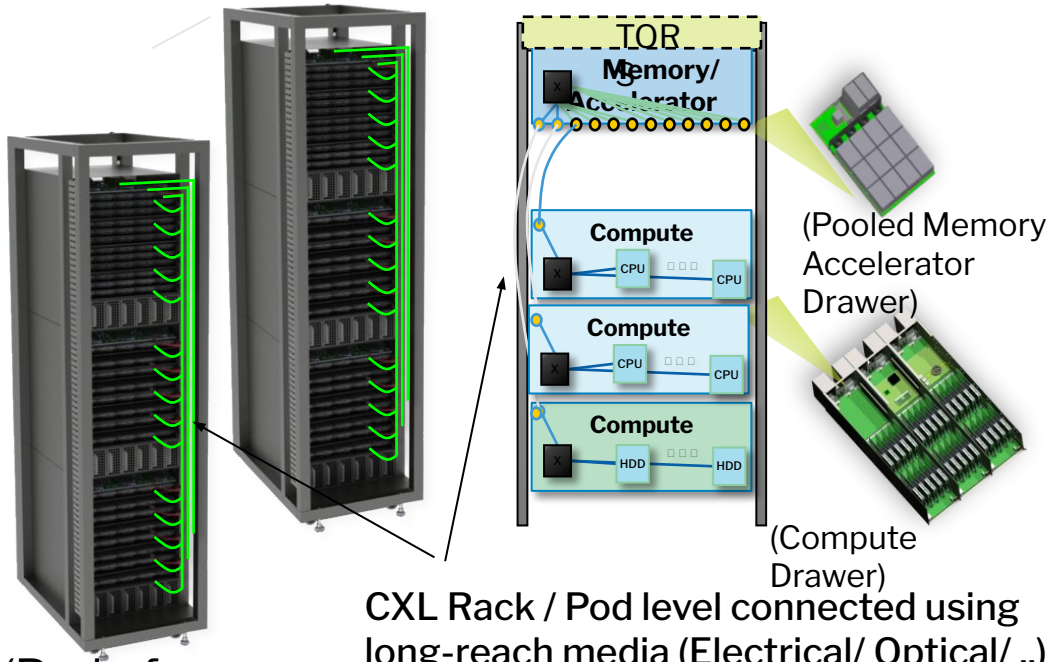


Remote Memory with UCIe Optical

UCIe Usage: Off-Package Connectivity with UCIe Retimers



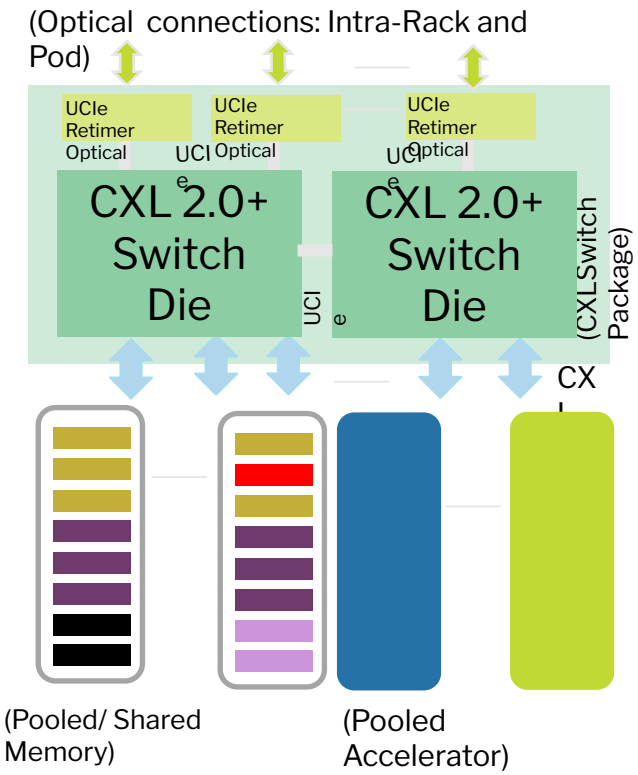
(Vision: Load-Store I/O (CXL) as the fabric across the Pod providing low-latency and high bandwidth resource pooling/ sharing as well as message passing)

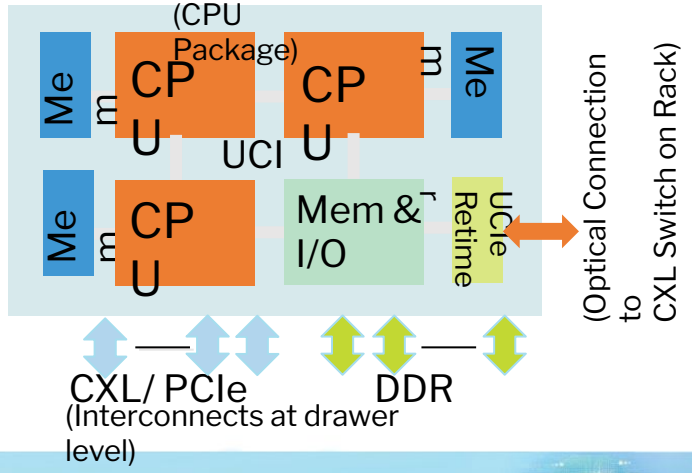


(Pod of Racks)

CXL Rack / Pod level connected using long-reach media (Electrical/ Optical/ ..) through UCIe Retimers (e.g., co-packaged optics)

(Physical Connectivity using UCIe-Retimer based co-packaged optics)





- Rack/ Pod Level resource pooling/ sharing with UCIe

UCIe 1.0: Characteristics and Key Metrics

CHARACTERISTICS	STANDARD PACKAGE	ADVANCED PACKAGE	COMMENTS
Data Rate (GT/s)	4, 8, 12, 16, 24, 32		Lower speeds must be supported -interop (e.g., 4, 8, 12 for 12G device)
Width (each cluster)	16	64	Width degradation in Standard, spare lanes in Advanced
Bump Pitch (um)	100 – 130	25 - 55	Interoperate across bump pitches in each package type across nodes
Channel Reach (mm)	<= 25	<=2	

KPIs / TARGET FOR KEY METRICS	STANDARD PACKAGE	ADVANCED PACKAGE	COMMENTS
B/W Shoreline (GB/s/mm)	28 – 224	165 – 1317	Conservatively estimated: AP: 45u; Standard: 110u; Proportionate to data rate (4G – 32G)
B/W Density (GB/s/mm^2)	22-125	188-1350	
Power Efficiency target (pJ/b)	0.5	0.25	
Low-power entry/exit latency	0.5ns <=16G, 0.5-1ns >=24G		Power savings estimated at >= 85%
Latency (Tx + Rx)	< 2ns		Includes D2D Adapter and PHY (FDI to bump and back)
Reliability (FIT)	0 < FIT (Failure In Time) << 1		FIT: #failures in a billion hours (expecting ~1E-10) w/ UCIe Flit Mode

UCIe 1.0 delivers the best KPIs while meeting the projected needs for the next 5-6 years.
Wide industry leader adoption spanning semiconductor, manufacturing, assembly, & cloud segments.

Future Directions and Conclusions

- Chiplets and D2D interface are essential to the compute continuum
  - Power-efficient performance, yield optimization, different functions, custom solutions, cost-effective

- UCIe standardization will propel the development an open ecosystem
  - Open plug-and-play “slot” at package level will unleash innovations
  - Evolution needs to track the underlying packaging technology to deliver compelling metrics
  - Form-factor, New Protocols, and manageability are some other areas for innovation

- The open chiplet journey with UCIe just started! Join us in what will be an exciting journey for decades!